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(delay or latency) + (bypass or forward) + (swi

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DJ Friedman, M Meghelli, BD Parker, J Yang, H ... - IBM Journal of Research and Development, 2003 - research.ibm.com

... are also used for feedback and **bypass** capacitors ... of the phase detector (PD) reduces loop **latency** and thus ... Reasonable **delay** mismatch (a few picoseconds) will not ...

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High-level Optimization of Pipeline Design

JPL Campbell, NA Day - High-Level Design Validation and Test Workshop, 2003. Eighth ..., 2003 - cs.toronto.edu

... We can then **forward** the value back from MEM to ID. ... In addition to the **bypass**, ... the 2 instructions. Stalls **delay** the processing of instructions. ...

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SiGe BiCMOS integrated circuits for high-speed serial communication

MB Ritter, L Shan, SJ Zier, M Sorna, M Soyuer - research.ibm.com

... well as SONET rates with significant **forward** error correction ... also used for feedback and **bypass** capacitors ... single out-of-tolerance measurements **switch** the RxPLL ...

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DYNAMIC INSTRUCTION SCHEDULER DESIGNS FOR POWER AND COMPLEXITY-AWARE MICROPROCESSORS

J SHARKEY - cs.binghamton.edu

... and SPICE simulations of the issue queues are used to estimate **delay**, energy, and area ... OF INSTRUCTIONS WHOSE LAST ARRIVING PARENT HAS A SINGLE - CYCLE **LATENCY** ...

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D Hormdee - cs.man.ac.uk

... 165 Figure 8.15 **Latency** distribution 166 ... The advantage of this approach is that the timing constraints for correct operation of the **circuit** (ie that the ...

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FET HBT, OC SERDES - doi.wiley.com

... capacitors are also used for feedback and **bypass** capacitors. ... transceiv- er), a clock is fed **forward** from the ... Since the total **delay** in this loop, comprising of ...

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... A.5 - Address Comparator **Circuit**....281 ... A.11 - Control Flag **Multiplexer** Values. ...

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... are also used for feedback and **bypass** capacitors. ... is just below 40 Gb/s. Once **forward-error-correction** ... in order to confirm their functionality at full **speed**. ...

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... as well as SONET rates with significant **forward** error correction ... are also used for feedback and **bypass** capacitors. ... The high-speed portion of the **circuit** uses ...

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... as well as SONET rates with significant **forward** error correction ... are also used for feedback and **bypass** capacitors. ... Since the high-speed part of the IC is fully ...

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... 2 Execution **Speed**.....226 ... of East **Skip** Bus ... Flag **Multiplexer** ...

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P DataSheet - techwellinc.com

... one time and allow the software to **switch** between them ... those produced by VCR duringfast **forward**, rewind or ... channels have built-in clamping **circuit** that restore ...[View as HTML](#) - [Web Search](#) - [synctechonology.co.kr](#) - [ic-land.com](#) - [synctechonology.co.kr](#)Design Compiler

SR Manual - 1997 - informatik.uni-jena.de

... 4-7 Optimization **Switch** Default Settings. 9-3 Saving (**Forward**-Annotating) DelayData 11-19 Reporting a Carry-**Bypass** Adder as the Longest PathCited by 1 - [View as HTML](#) - [Web Search](#) - [ece.northwestern.edu](#) - [emba.uvm.edu](#) - [ece.northwestern.edu](#) - [all 5 versions »](#)LEADING-EDGE APPLICATIONS

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PU Verilog - jwdt.com

... 34 6.5 Stack **bypass** four topmost values of other stacks through a four way crossbar**switch**. ... and less important, using command line defined macros to **skip** them ...[View as HTML](#) - [Web Search](#)Wormhole run-time reconfiguration: conceptualization and VLSI design of a high performance computing

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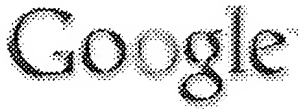
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[SiGe BiCMOS integrated circuits for high-speed serial ...](#) - by Friedman - 2 citations

[High-level Optimization of Pipeline Design](#) - by Campbell - 0 citations

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Michael Barr's Embedded Systems Glossary

Butterworth filter, button, Buy versus build, **bypass** capacitor, byte ... data plane,
data segment, data **selector**, data sheet, data terminal ready ...

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[PDF] High-level Optimization of Pipeline Design

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pipelines there may be multiple **bypass**, stall, kill or **selector** units. ...

library components include an ALU, a pipeline register, and a **multiplexer (MUX)**. ...

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Figure 19 gives a qualitative comparison of the **multiplexer (MUX)** ... of this
architecture are the **delay** matching between A1 and the **selector** of D3, ...

researchweb.watson.ibm.com/journal/rd/472/friedman.html - 110k - Sep 20, 2005 - [Cached](#) - [Similar pages](#)

Sybex Encyclopedia of Networking

... NIC; Cable; Dual **Bypass Switch**; Connectors; Concentrators; ... **Latency**; Layer; Layer
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The **bypass** operation occurs In a single **multiplexer**. **delay** even for multiple row

... **mux**. = 0.98 ns. The resulting approximate average **latency** of The whole ...

[vlsi.die.uniroma1.it/publishing/ variable-latency-multiplier-major-revision'per'web.pdf](http://vlsi.die.uniroma1.it/publishing/variable-latency-multiplier-major-revision'per'web.pdf) - Supplemental Result - [Similar pages](#)

United States Patent Application: 0050131987

... **forward** scheme is the increased **latency** penalty introduced and incurred by each

... the **bypass selector** or **multiplexer** 608 may also be referred to as a ...

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Data Communication Glossary

block **Multiplexer** Channel - an IBM term used to describe A computer peripheral

... Data PBX - A digital transmission **Circuit switch** allowing users to select ...

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